JJMICROELECTRONICS

100V, 61A, 5.9mΩ N-channel Power SGT MOSFET JMSH1006PK

Features

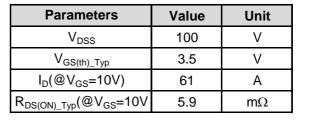
- Excellent $\mathsf{R}_{\mathsf{DS}(\mathsf{ON})}$ and Low Gate Charge

D

- 100% UIS Tested
- 100% ΔVds Tested
- Halogen-free; RoHS-compliant

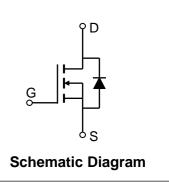
Applications

- Load Switch
- PWM Application
- Power Management





Product Summary



Ordering Information

TO-252-3L

Device	Marking	MSL	Form	Package	Reel(pcs)	Per Carton (pcs)
JMSH1006PK	SH1006P	3	Tape&Reel	TO-252-3L	2500	25000

Pin Assignment

Absolute Maximum Ratings (@ T_c = 25°C unless otherwise specified)

Symbol	Parameter		Value	Unit
V _{DS}	Drain-to-Source Voltage	Drain-to-Source Voltage		V
V _{GS}	Gate-to-Source Voltage		±20	V
	Continuous Drain Current	$T_C = 25^{\circ}C$	61	А
Ι _D	Continuous Drain Current	$T_{\rm C} = 100^{\circ}{\rm C}$	38	A
I _{DM}	Pulsed Drain Current ⁽¹⁾		Refer to Fig.4	A
E _{AS}	Single Pulsed Avalanche Energ	3y ⁽²⁾	356	mJ
PD	Dower Dissinction	$T_C = 25^{\circ}C$	50	W
' D	Power Dissipation	$T_{\rm C} = 100^{\circ}{\rm C}$ 20	20	VV
T _J , T _{STG}	Junction & Storage Temperature	Range	-55 to 150	°C

Thermal Characteristics

Symbol	Parameter	Мах	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient ⁽³⁾	65	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction to Case	2.5	0/10

Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
Off Cha	aracteristics					
V _{(BR)DSS}	Drain-Source Breakdown Voltage	$I_{D} = 250 \mu A, V_{GS} = 0 V$	100	-	-	V
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80V, V_{GS} = 0V$	-	-	1.0	μA
I _{GSS}	Gate-Body Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	±100	nA
On Cha	racteristics	•				
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2.5	3.5	4.6	V
R _{DS(ON)}	Static Drain-Source ON-Resistance ⁽⁴⁾	$V_{GS} = 10V, I_D = 20A$	-	5.9	7.6	mΩ
Dynam	ic Characteristics					
R_g	Gate Resistance	f = 1MHz	-	0.6	-	Ω
C _{iss}	Input Capacitance		2246	3144	4245	pF
C _{oss}	Output Capacitance	$V_{GS} = 0V, V_{DS} = 50V,$ f = 1MHz	336	470	634	pF
C _{rss}	Reverse Transfer Capacitance		13	19	25	pF
Qg	Total Gate Charge		36	51	69	nC
Q_{gs}	Gate Source Charge	$V_{GS} = 0 \text{ to } 10V$ $V_{DS} = 50V, I_D = 20A$	12	17	23	nC
Q_gd	Gate Drain("Miller") Charge	VDS = 0000, 10 = 2010	9	12	16	nC
Switchi	ing Characteristics					
t _{d(on)}	Turn-On DelayTime		-	15	-	ns
t _r	Turn-On Rise Time	V _{GS} = 10V, V _{DD} = 50V	-	18	_	ns
t _{d(off)}	Turn-Off DelayTime	I_{D} = 32A, R_{GEN} = 2.7 Ω	_	27	_	ns
t _f	Turn-Off Fall Time		-	8	-	ns
Body D	iode Characteristics	-		<u> </u>	ļ	1
I _S	Maximum Continuous Body Diode Forward	Current	-	-	61	Α
I _{SM}	Maximum Pulsed Body Diode Forward Current		-	-	243	A
V_{SD}	Body Diode Forward Voltage	$V_{GS} = 0V, I_{S} = 20A$	-		1.2	V
trr	Body Diode Reverse Recovery Time		40	56	76	ns
Qrr	Body Diode Reverse Recovery Charge	I _F = 15A, di/dt = 100A/us	-	106	-	nC

Electrical Characteristics ($T_J = 25^{\circ}C$ unless otherwise specified)

Notes: 1. Repetitive Rating: Pulse Width Limited by Maximum Junction Temperature.

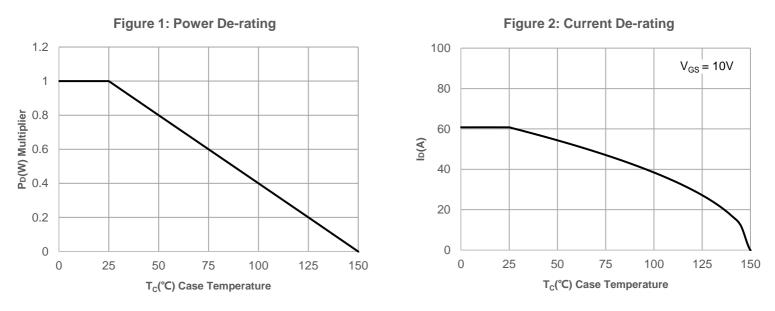
2. E_{AS} condition: Starting T_J =25C, V_{DD} =50V, V_G =10V, R_G =250hm, L=3mH, I_{AS} =15.4A, V_{DD} =0V during time in avalanche.

3. R_{BJA} is measured with the device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.

4. Pulse Test: Pulse Width ${\leqslant}300\mu\text{s},$ Duty Cycle ${\leqslant}0.5\%.$







Typical Performance Characteristics



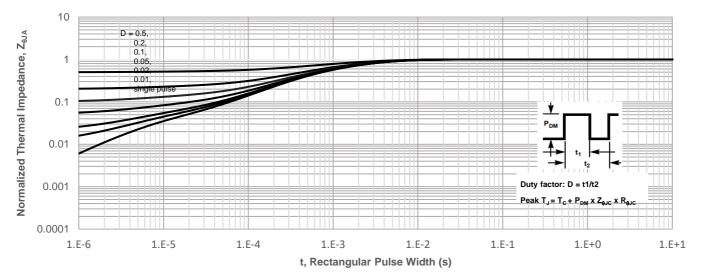
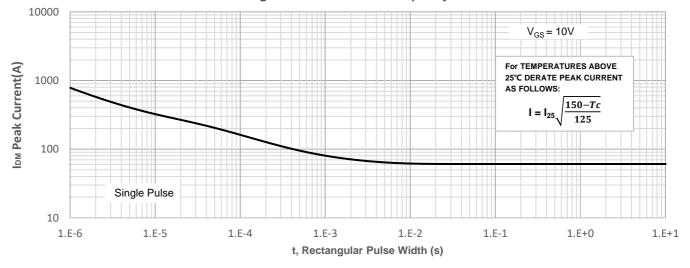
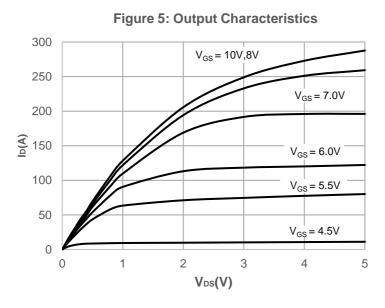


Figure 4: Peak Current Capacity







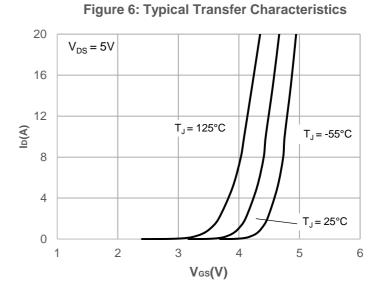


Figure 8: Body Diode Characteristics

100

10

1

0.1

0.01

0

0.2

Is(A)

 $V_{GS} = 0V$

T_J = 125°C

Figure 7: On-resistance vs. Drain Current 13.00 12.00 11.00 10.00 9.00 $V_{GS} = 10V$ $R_{DS(ON)}(m\Omega)$ 8.00 7.00 6.00 5.00 4.00 3.00 2.00 1.00 0.00 0 5 10 15 20 ID(A)

Figure 9: Gate Charge Characteristics

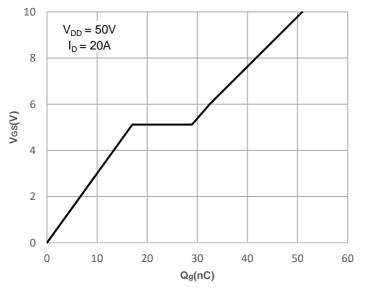


Figure 10: Capacitance Characteristics

0.8

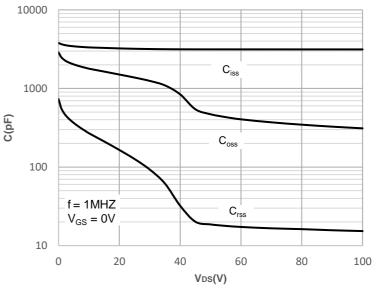
0.6

Vsd(V)

T_J = -55°C

1

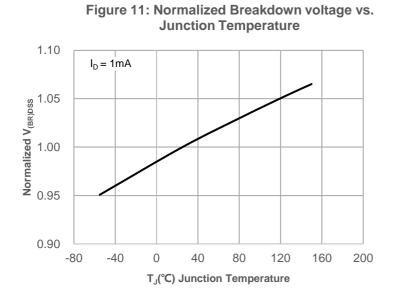
1.2



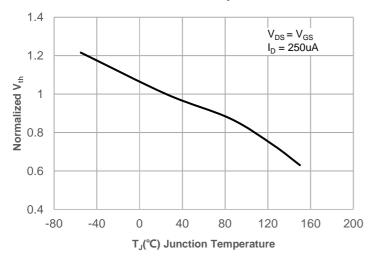
 $T_1 = 25$

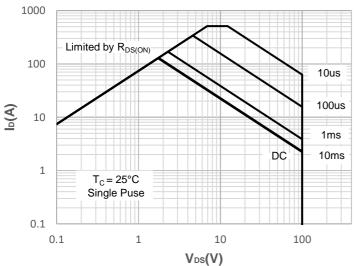
0.4

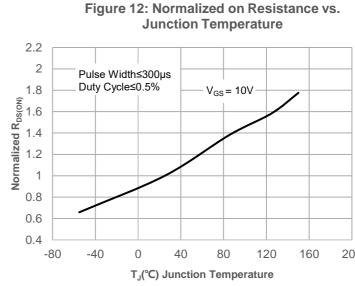
Typical Performance Characteristics

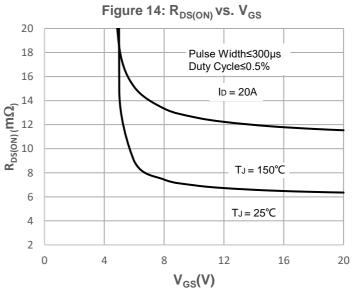


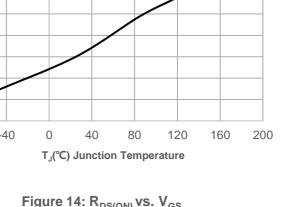












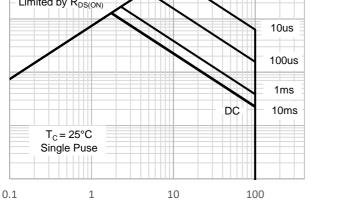


Figure 15: Maximum Safe Operating Area

Test Circuit

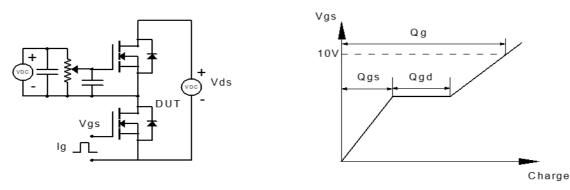


Figure 1: Gate Charge Test Circuit & Waveform

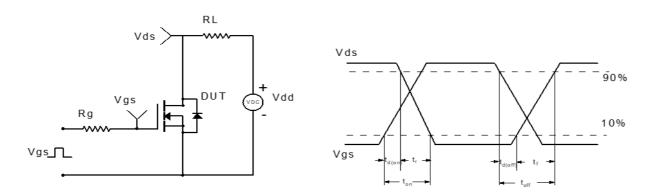


Figure 2: Resistive Switching Test Circuit & Waveform

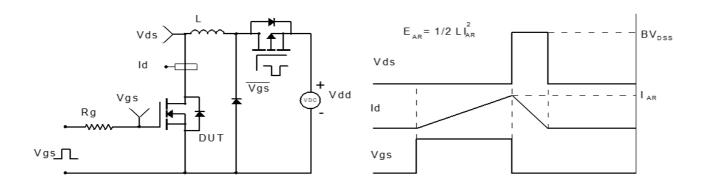


Figure 3: Unclamped Inductive Switching Test Circuit& Waveform

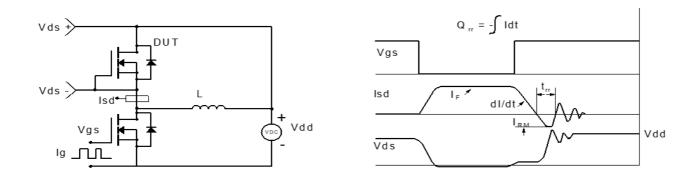
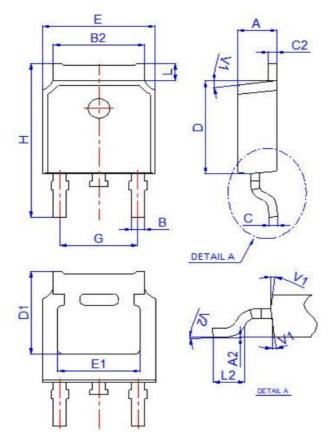


Figure 4: Diode Recovery Test Circuit & Waveform

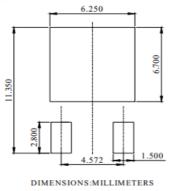


Package Mechanical Data(TO-252-3L)



Ref.			Dime	ensions				
	Millimeters			Inches				
	Min.	Тур.	Max.	Min.	Тур.	Max.		
A	2.10		2.50	0.083		0.098		
A2	0	8	0.10	0	Ċ.	0.004		
В	0.66		0.86	0.026		0.034		
B2	5.18		5.48	0.202		0.216		
С	0.40		0.60	0.016		0.024		
C2	0.44		0.58	0.017		0.023		
D	5.90		6.30	0.232		0.248		
D1	5.30REF			C	.209RE			
E	6.40		6.80	0.252		0.268		
E1	4.63			0.182				
G	4.47		4.67	0.176		0.184		
Н	9.50		10.70	0.374		0.421		
L	1.09		1.21	0.043		0.048		
L2	1.35		1.65	0.053		0.065		
V1		7°			7°			
V2	0°		6°	0°		6°		

Recommended Soldering Footprint



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